ON-CHIP PULSE TRANSMISSION IN VERY HIGH SPEED LSI/VLSIS

Hideki Hasegawa and Shouhei Seki

Department of Electrical Engineering,

Faculty of Engineering,

Hokkaido University, Sapporo, 060 Japan

ABSTRACT

Using single and coupled metal- insulator-semiconductor (MIS) microstrip line models for interconnection, on-chip pulse delay and crosstalk in very high-speed LSI/VLSIs, are analyzed. The result shows (1) inapplicability of lumped capacitance approximation for interconnection in very high-speed LSI/VLSIs($t_{pd} < 100$ ps), (2) superiority of semi-insulating substrates over semi-conducting substrates, (3) importance of driving capability of device to achieve high speeds at LSI/VLSI level and (4) importance of crosstalk in interconnection design.

INTRODUCTION

There exist ever increasing demands for very high speed integrated circuits in areas of high-speed computation, signal processing, data links and related instrumentation, where LSIs with the propagation delay per gate t_{pd} below 100 ps are required. In SSI/MSI integration level, propagation delay time per gate reaching 10ps range has already been realized with various technologies. However, the on-chip interconnection delay can be a serious problem in very high speed LSI/VLSIs, and a proper design considerations to minimize it should be paid in order to take full advantage of the inherent speed capability of the device.

The average interconnection length on LSI/VLSI chips is known to increase with the gate count G as G^{α} with $\alpha=0.2$ - 0.6, and becomes 0.5 - 5 mm for G = 10^3 - 10^4. Thus, speed is limited not only by device itself, but by the fact that each gate should drive interconnections sufficiently quickly. Previously, this effect has been treated in terms of the "lumped capacitance" of interconnections. However, since the propagation time of an ideal TEM wave over 1 mm distance is typically 8-10 ps on a semiconductor substrate (ε_r= 12-13), validity of such an approach becomes very doubtful in high-speed LSI/VLSIs.

The purpose of the present paper is to investigate the transmission line effects of interconnections in very high-speed integrated circuits. On-chip propagation delay and crosstalk are analyzed, using single and coupled microstrip line models loaded with lossy or lossless semiconductor substrates. The result shows that interconnections should be treated as miniaturized microwave networks in the design of LSI/VLSIs with t_{pd} below 100 ps.

SINGLE AND COUPLED MIS MICROSTRIP LINE MODEL

Models and Approach

Single and coupled MIS(metal-insulator-semiconductor) microstrip line models shown in Fig.1 were employed in order to study the effects of the conductivity of semiconductor substrates on pulse transmission. Rigorous analysis of such models is obviously extremely complicated and can only be done numerically in frequency domain either by the spectral domain method [1] or by the finite element method [2]. However, these complicated

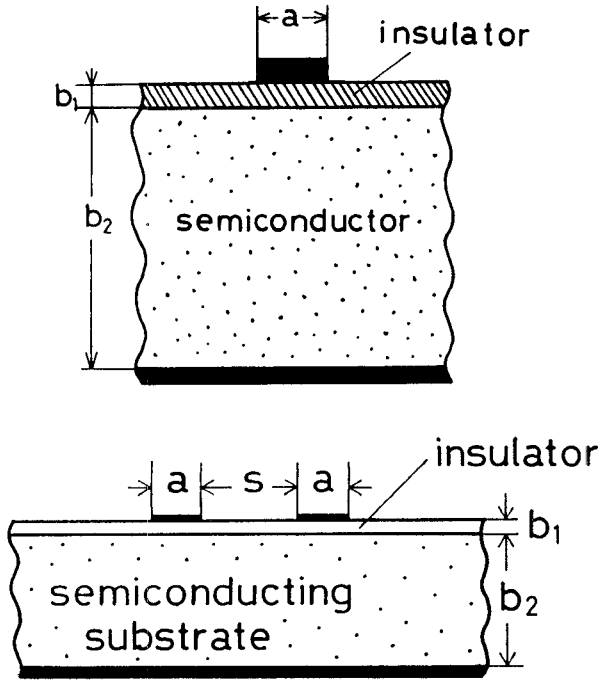


Figure 1. Single and coupled MIS microstrip line models used in the present study.

CH2042-0/84/0000-0029 $1.00

numerical procedures, which sometimes find difficulties in obtaining proper convergence, are not practical for time domain analysis. The equivalent circuit approach by the present authors [3,4] was employed here for the time domain analysis.

Derivation of Equivalent Circuit

In order to improve the accuracy in treating the skin effect in semiconductor under the finite-width microstrip as compared with our previous analysis[3,4], an improved equivalent circuit was derived in the following way. In the low-frequency limit, the fields are determined by Laplace's equation. The single microstrip line in Fig.1 was mapped to the inhomogeneous parallel-plate waveguide with a closed boundary shown in Fig.2 through a suitable Schwarz-Cristoffel(S-C) transformation. In order to include the skin effect, transformation of the Helmholtz's equation for E_z is considered. Although Helmholtz's equation is in general variant under a S-C transformation, it can be regarded invariant in the vicinity of the underneath of the strip provided that appropriate values are assigned to the scaling parameter of S-C transformation and to the effective longitudinal conductivity to be used in the transformed domain. This allows us to use the result of the parallel-plate waveguide analysis [3] in the transformed domain for the evaluation of the semiconductor impedance $Z_s(\omega)$. The resulting equivalent circuit per unit length is shown in Fig.3.

Using a similar procedure, equivalent circuits

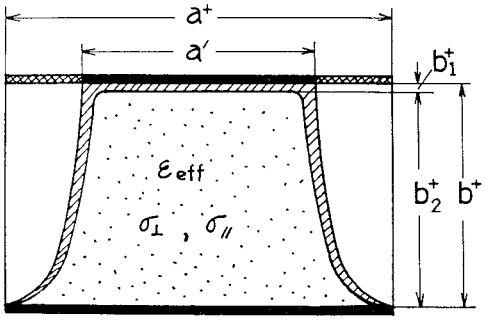


Figure 2. Inhomogeneous parallel-plate waveguide obtained by a S-C transformation of single microstrip line model in Fig.1.

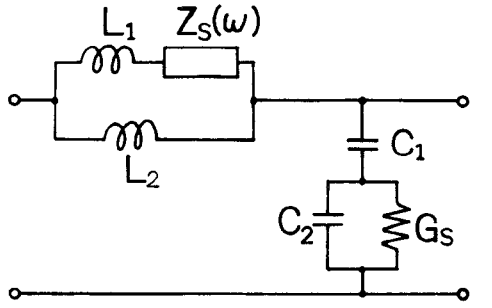


Figure 3. Equivalent circuit per unit length of the single MIS microstrip line.

were obtained for odd and even modes for the coupled microstrip line model shown in Fig.1. For this purpose, mapping was carried out based on the work done by Akhtarzad et al[5].

Frequency Domain Analysis

In order to check the validity of the present approach, transfer characteristics in frequency domain, calculated using the equivalent circuit shown in Fig.3, are compared with the results of the numerical analyses [1,2] and with our previous experimental data[3]. Plots of the slow-wave factor are shown in Fig.4. Agreement is good particularly with the result by the finite element method. The experimentally observed attenuation constant was found to be somewhat higher than theoretical values, and this is presumably due to the metallic loss which is not considered in theory.

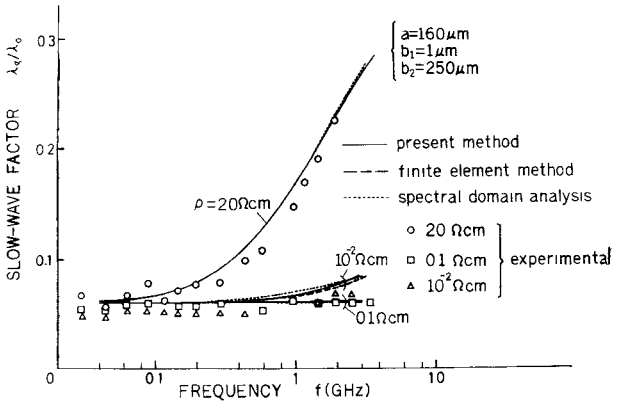


Figure 4. Comparison of slow-wave factors obtained by present and other theories and experiment.

INTERCONNECTION DELAY

Matched Termination

Fig.5 shows the calculated propagation delay time (time to 50% rise) and the rise time (10-90% rise) of the step response as a function of the semiconductor substrate resistivity. The single microstrip line model was used. The response is calculated at positions with distance of z = 1 and 3 mm from the signal source. The interconnection length is assumed to be semi-infinite or the line is assumed to be terminated with a matched load. The behavior of the delay and rise times vs. substrate resistivity can be explained in terms of the three fundamental modes, i.e., the dielectric quasi-TEM mode, slow-wave mode and skin-effect mode[3]. Increase of delay time at mid-resistivity range is due to the slow-wave mode, and rise time peaks on both sides of the delay time peak is due to mode transition from the slow-mode either to the dielectric quasi-TEM mode or to the skin-effect mode. It should be noted that considerable deterioration of pulse response takes place at resistivities of 1 - 10 ohm-cm, which are frequently used in Si technology.

Interconnections Between Logic Gates

The present model was further applied to the situation where two gates are connected by an

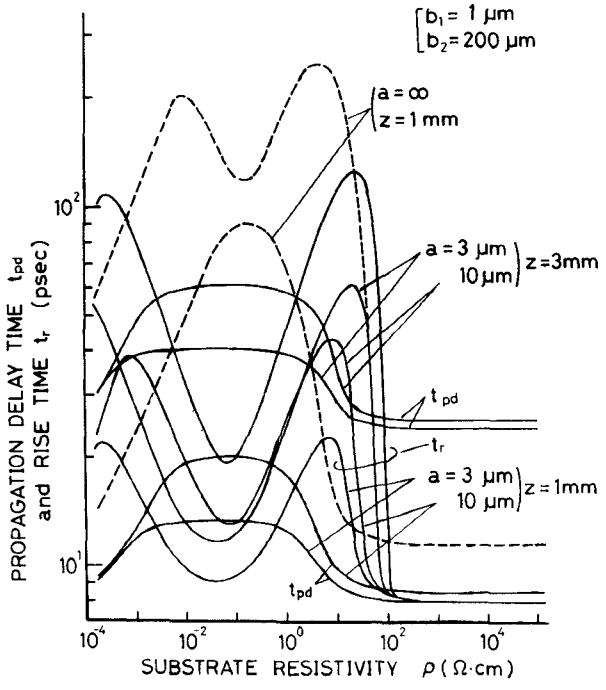


Figure 5. Calculated propagation delay time and rise time of the step response.

interconnection as shown in Fig.6(a). For the calculation, the gate output was represented by its effective signal source resistance R_S, and the gate input was represented by an input capacitance C_L as shown in Fig.6(b). It can be shown that, in the gates consisting of FET devices such as MOSFETs, MESFETs and HEMTs, R_S is approximately equal to the inverse of the transconductance g_m of the transistor taking part in the transient. The calculated step response is shown vs. R_S of the

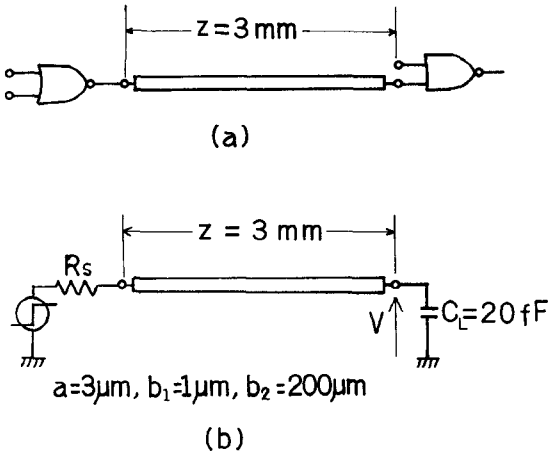


Figure 6. (a)Interconnection between two gates and (b) its model.

gate in Fig.7 (a) and (b) in terms of the propagation delay time t_{pd} and the rise time as observed at the input of the second gate. The parameter is the substrate resistivity in ohm-cm. The step response as obtained by the lumped capacibtance approximation of interconnection is also shown by the two dashed lines, one being the case in which the semiconductor substrate is assumed to be a perfect conductor ($\rho = 0$), and the

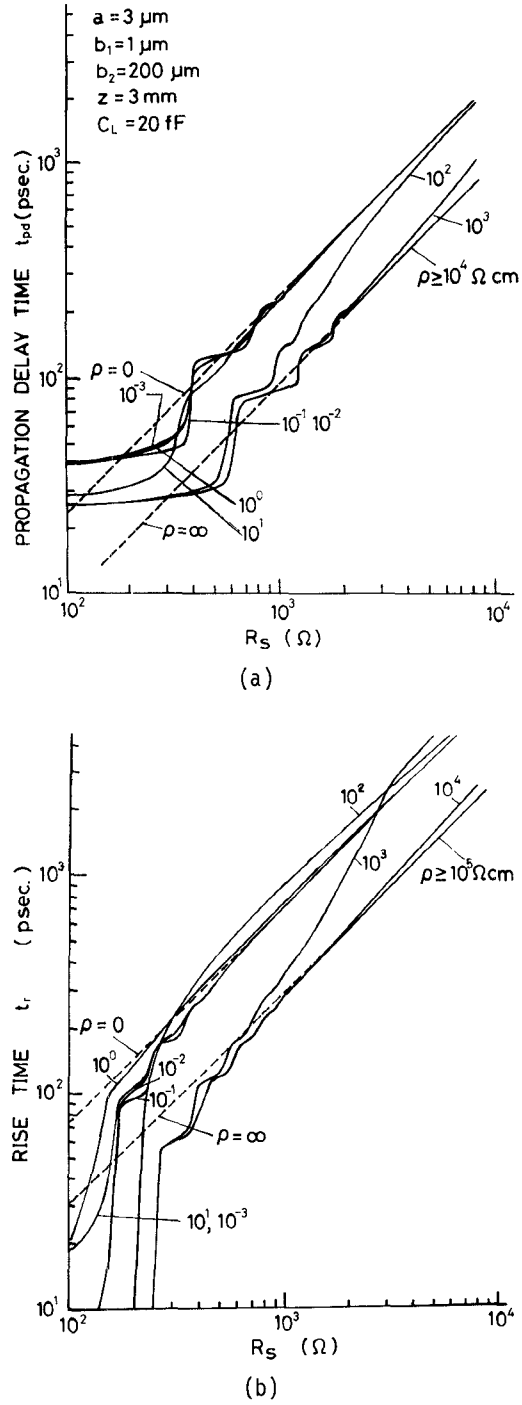


Figure 7. (a) Calculated propagation delay time and (b)rise time vs. R_S of the gate.

other, the case in which it is assumed to a perfect insulator($\rho = \infty$). It is clear from the present result that lumped capacitance approximation cannot be used in LSI/VLSIs with t_{pd} below 100 ps. It also seen that strong driving capability of device is essential in realizing very high-speed LSI/VLSIs. In the typical E/D type gates with E device having gate length of 1 μm and width of 10 μm, R_s of the E device is 100-200 ohms for HEMT, 300-500 ohms for GaAs MESFET and 1000-1500 ohms for Si MOSFET. Additionally it should be noted that R_s of the depletion load is usually 4-5 times larger than that of the E device, thereby limiting the response speed more severely in the turn- off transient. Fig.6 also shows that semi-insulating substrates offer significant advantages for high-speed pulses. Larger driving capability of device is required in semi-conducting substrates.

CROSSTALK

Coupled MIS Microstrip Line Model

The calculated step response waveforms using the coupled microstrip line model in Fig.1, are shown together with the excitation conditions. The parameter is the substrate resistivity. It is seen that large crosstalks take place between two adjacent interconnections, with their polarities changing with resistivity. When the resistivity is high, capacitance coupling dominates, while inductance coupling dominates when the resistivity is low. The lumped capacitance approximation predicts smaller crosstalk for conductive substrates[6]. However, this is not the case if transmission line effects are included. The crosstalk becomes minimum at resistivity of about 1-10 ohm-cm, but the response in the active line also becomes slowest.

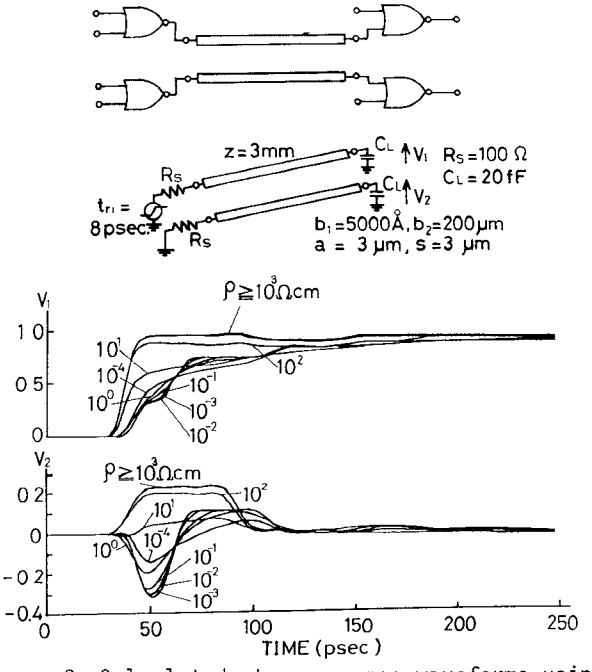


Figure 8. Calculated step response waveforms using coupled MIS microstrip line model. Excitation conditions are shown on the top.

Periodic Multi-Conductor MIS Microstrip Lines

In order further to analyze complicated crosstalk phenomenon, the coupled multi-conductor microstrip line model shown in Fig.9 was analyzed under the periodic excitation. For simplicity, loss in the semiconductor substrate was ignored. Mode impedances and propagation constants were determined using the periodic Green's function. Then, crosstalk voltages were evaluated in time domain for various loading and excitation conditions, using a superposition of forward and backward waves of line current and voltage of each mode. When interconnections are excited periodically with the period of n conductors, (n-1) modes must be included. Fig.10 shows the calculated coupling coefficients for semi-infinite interconnections running parallel with n = 4. Actual crosstalk waveforms for the excitation conditions shown in Fig.11(a) are shown in Fig.11(b). It is seen that crosstalk is greatly reduced by placing neighboring ground lines, but it also reduces the response speed of the active line. It is also noted that the actual crosstalk amplitude is different from the coupling coefficients in Fig.10 and dependent on the excitation condition.

Thus, crosstalk can be a very serious problem in high-speed LSI/VLSIs. Use of ground lines for shielding is effective to a certain extent, but it

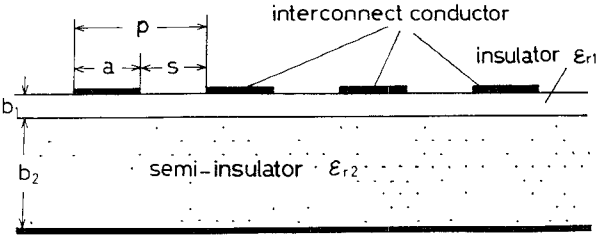


Figure 9. Multi-conductor MIS microstrip line model for crosstalk analysis.

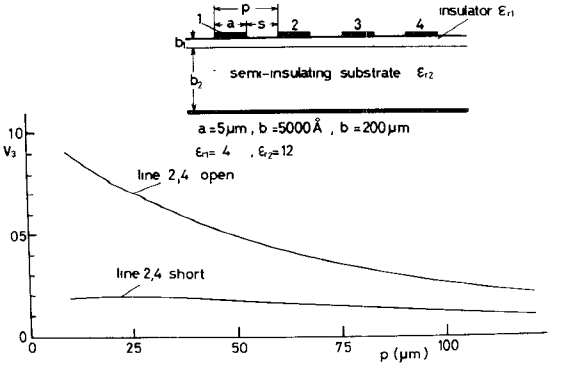
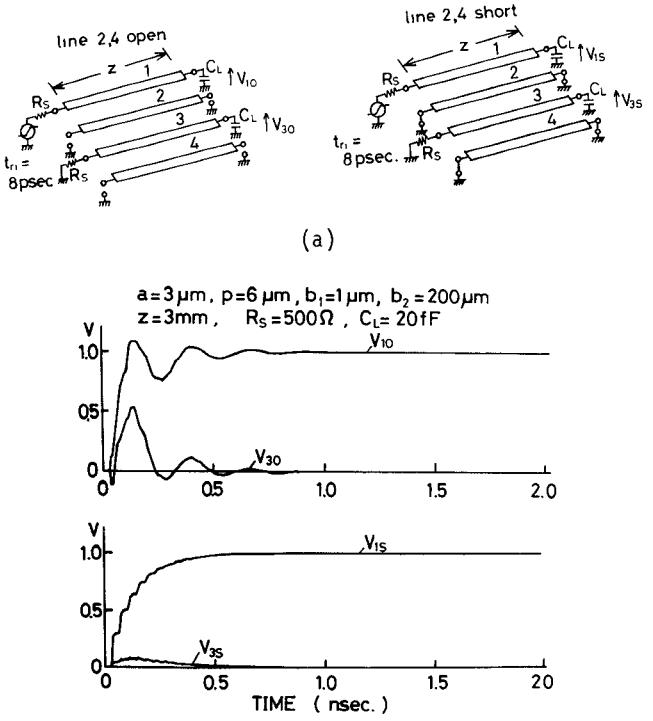


Figure 10. Calculated coupling coefficients vs.pitch (n = 4).

can cause unwanted ringing under certain circumstances. Additionally, it will severely limit the capacity of the wiring channel and tends to increase both chip size and interconnection length. An alternative shielded multi-level planar interconnection scheme is shown in Fig.12. This seems to reduce crosstalk and simplify interconnect layout and timing design with the use of standard strip line theory.



(a)

(b)

Figure 11. (a)Excitation conditions and (b)calculated transient waveforms under these conditions.

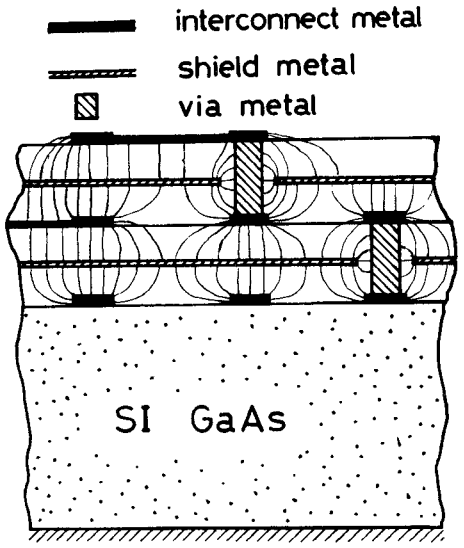


Figure 12. Shielded multi-level planar interconnect scheme for reduced crosstalk and simplified layout and timing designs in high-speed regime.

CONCLUSION

On-chip pulse delay and crosstalk on interconnections of very high speed LSI/VLSIs are investigated using MIS microstrip line models. Main conclusions of the present study are the following:

(1)Lumped capacitance approximation of interconnections cannot be used in LSI/VLSIs with t_{pd} below 100ps. Microwave considerations are required in the logic, circuit and layout design of such very high speed integrated circuits.

(2)Driving capability of device per unit layout area is essentially important for high-speed LSI/VLSIs. Heterojunction bipolar transistors (HBT) and HEMT seem promising, although their reported performances are not still sufficient to drive long interconnections at a high speed.

(3)Semi-insulating property of substrates offers significant advantages for high-speed pulse transmission in LSI/VLSIs. Semi-conducting substrates suffer from slow-wave mode, mode transition and strong inductive coupling, and require higher drive capability of devices for high-speed operation.

(4)Crosstalk can be a serious problem in high-speed LSI/VLSIs. Insertion of ground lines beside the active line reduces the crosstalk, but the dynamic ringing has to be considered. An alternative shielded multi-level planar interconnect scheme is proposed.

REFERENCES

[1]P.Kennis and L.Faucon,"Rigorous analysis of planar MIS transmission lines",Electron. Lett. vol.17,no.13,pp.454-456,June 1981.

[2]M.Aubourg,J-P.Villotte,F.Godon and Y.Garaut, "Finite element analysis of lossy waveguides - application to microstrip lines on semiconductor substrates",IEEE Trans. Microwave Theory & Tech.,vol.MTT-31,pp.326-330,April 1983.

[3]H.Hasegawa,M.Furukawa and H.Yanai,"Properties of microstriplines on Si-SiO_2 system,"IEEE Trans. Microwave Theory & Tech. vol.MTT-19,pp.869-881,Nov. 1971.

[4]S.Seki and H.Hasegawa, "Pico-second pulse response of interconnections of high-speed GaAs and Si LSIs",Tech. digest of the 1982 GaAs IC Symp.,New Orleans,Nov. 9-11,1982.

[5]S.Akhtarzadm T.R.Rowbothan and P.B.Jones,"The design of coupled microstrip lines",IEEE Trans.Microwave Theory & Tech. vol.MTT-23, pp.486-492,June 1975.

[6]H-T Yuan,Y-T Lin and S-Y Chiang,"Properties of interconnection on silicon, sapphire and semi-insulating gallium arsenide substrates", IEEE Trans. Electron Devices, vol.ED-29,pp.639-644,April 1982.